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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
RAYNOR ET AL.

Serial No. **09/993,387**

Filing Date: **November 16, 2001**

For: **SOLID STATE IMAGING DEVICE AND ASSOCIATED METHODS**

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Respectfully submitted,

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16NOV00 E584113-9 D02884
P01/7700 0.00-0027931.5

1. Your reference	P26562-/TSI/JCO
2. Patent Application Number *(the Patent Office will fill in this part)*	**0027931.5**
3. Full name, address and postcode of the or of each applicant *(underline all surnames)*	STMicroelectronics Ltd Aviation House 31 Pinkhill EDINBURGH EH12 7BF
Patents ADP number *(if you know it)*	8022873001
If the applicant is a corporate body, give the country/state of its incorporation	United Kingdom
4. Title of the invention	"Solid State Imaging Device"
5. Name of your agent *(if you have one)*	Murgitroyd & Company
"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	373 Scotland Street GLASGOW G5 8QA
Patents ADP number *(if you know it)*	1198013

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"Solid State Imaging Device"

This invention relates to a solid state imaging device which can be operated to provide an improved shutter function.

There are various basic CMOS pixel structures. One common type, with 3 transistors per pixel, is described in US 4,407,010 ("CMOS 3T" pixel), illustrated in Fig. 1 of the accompanying drawings. This is an efficient structure as a transistor M1 amplifies the photodiode output inside the pixel. Transistor M2 serves to reset the voltage on the pixel. Transistor M3 is a multiplex transistor - it enables many pixels in a column to be wired together and only one pixel enabled at a time. The device "Iload" is typically a sense amplifier which both provides a load for the source follower transistor M1 and also measures the output voltage.

The typical voltage on a photodiode is shown in Figure 2. At point "1", the pixel is reset by turning on transistor M2 which sets the voltage on the reverse-biased diode to a preset voltage (VRT). After this point, light falling onto the pixel will create photo-generated electrons which will be attracted to the photodiode. This will cause the diode to be discharged. The amount of discharge is proportional to both the amount of light and also the amount of time. After a period of time (integration period, "Tint") the voltage on the pixel is measured. If the time "Tint" is kept constant, the swing will be proportional solely to the amount of light falling on the pixel.

Typically, as shown in Figure 3, the pixels are arranged into a 2-dimensional grid of rows and columns. There is one "Iload"/sense amplifier per column. The amplifier measures the output voltage of the pixel. Several (usually all pixels in a column) share a single sense amplifier. Because of this structure all the elements in a row are read out simultaneously (into the sense amplifiers) and the rows are addressed sequentially.

As the rows are read out sequentially, they must also be reset sequentially. This keeps the integration time "Tint", constant for the whole sensor, and the brightness of the image constant over the image plane.

This operation is called "rolling blade shutter" and is analogous to how a physical shutter in a 35mm SLR camera works. In the CMOS 3T sensor, the integration time is variable - this is achieved by varying the time between the reset and readout pulse. This is also similar to how 35mm SLR cameras work - the shutter blades move over the film at a constant rate, but a gap between the blades is adjusted to adjust the effective shutter speed.

Another common type of CMOS pixel has 4 transistors. There are various types of implementation, one of which is shown in Figure 4. The advantage of this design is that it has two storage capacitances per pixel. Cpd is formed by the "parasitic" capacitance of the photodiode. The storage node, Csn is formed partly by the stray capacitance of M1, M2 but also by creating a storage device inside the pixel. One advantage of a 4T pixel is sensitivity: V=Q/C; hence, by reducing the value of Csn, the output voltage for a given photocharge is increased.

The 4T pixel has another advantage - its ability to form an "electronic shutter". Although arrays of either 3T or 4T pixels can be reset simultaneously, the sequential readout mechanism of the 3T pixel prevents simultaneous readout. The 4T pixel does not suffer from this problem as it has a storage element incorporated inside each pixel ("Csn" in Figure 4). This permits the entire array to be "sensed" simultaneously, i.e. photo-generated charge is

transferred from each pixel's Cpd to the pixel's Csn simultaneously. The readout mechanism then proceeds in a row sequential fashion, similar to the mechanism used in 3T pixels. As all the pixels in the array are reset and measured simultaneously, the array captures a "snapshot" of the light pattern falling on the sensor (unlike the "rolling blade shutter" of 3T pixels). This technique is of great value for hand-held operation of the camera as the effect of camera shake is reduced as the total time for which the array is collecting light (as opposed to the time for which an individual pixel is collecting light) is minimised.

There are significant disadvantages with a 4T pixel:

- the extra circuitry (M4, Csn) occupies area on the pixel and this reduces the amount of light reaching the photodiode.
- transferring all the charge from Cpd to Csn is difficult to achieve. Special CMOS manufacturing techniques are often employed to change the structure of the photodiode Cpd or the transfer transistor M4. These manufacturing techniques are very costly (as they are non-standard) and are also difficult to achieve reliably.

There are also some "linear arrays" (see Figure 5) with two rows of pixels which have separate electronics on both top and bottom. These structures are limited to a maximum of two rows.

Other prior art in this area includes US 4,835,617, US 5,576,762, US 5,134,489, US 5,122,881, US 5,471,515 and WO 98/08079.

An object of the present invention is to provide a solid state image sensor which, like the 3T sensor, can be manufactured by standard techniques, but which also is capable of providing a true electronic shutter.

The invention and preferred features thereof are defined in the appended Claims.

Briefly stated, the invention is based upon locating the readout electronics off the image plane of the device. In preferred forms of the invention, this is facilitated by connecting each pixel to its associated readout electronics via a multi-conductor signal bus.

Embodiments of the invention will now be described, by way of example only, referring to the drawings in which:

Figures 1 to 5 illustrate the prior art discussed above;

Figure 6 shows a part of one column of an array structure embodying the invention;

Figure 7 is a timing diagram illustrating the operation of Figure 6;

Figure 8 shows a typical system layout of a sensor incorporating the circuitry of Figure 6;

Fig. 9 shows one pixel and read-out circuitry of a modified version of Fig. 6;

Figure 10 is a timing diagram illustrating the operation of Figure 9;

Figure 11 shows one pixel plus read-out circuitry of a further modification of Fig. 6;

Figure 12 is a timing diagram illustrating the operation of Figure 11;

Figure 13 is a view similar to Figure 8 but showing a modified system layout; and

Figure 14 shows a preferred readout arrangement for the circuit of Figure 11.

A basic feature of the invention is to provide a storage node per pixel and, to avoid degrading the fill factor (and hence light sensitivity), locating the storage element away from the image plane.

Referring to Figure 6, this embodiment has only two transistors, M1 and M2, per pixel, thus improving the

fill factor and sensitivity. The array is not multiplexed and therefore there is no mulitplex transistor in the pixel equivalent to M3 in Figure 1. Instead, there is a connection to the signal bus 10 which runs through the column.

The switches S2-1, S2-2 etc will typically be implemented as MOSFET transistors. The current loads Iload are to ensure correct operation of sense transistor M1. Figure 6 shows only two pixels, but in a practical array there are several pixels in a column.

The operation of the array is as follows. At point 1 (see Figure 7) the RST signal goes high, causing all the "M2" transistors (M2_1, M2_2 etc) to conduct and the voltage Vpix on the photodiode to be reset to Vrt. At a time later, point 2 (see Figure 7), all the "S1" switches (S1_1, S1_2 etc) are closed simultaneously and the output of the sense transistors (M1) are stored on the sense capacitors (Csn_1, Csn_2). Subsequently (not shown), the signals on the sense capacitors are readout sequentially by sequentially closing switches S2 (S2_1, S2_2 etc).

Figure 8 shows a typical layout of a system, with an image array 12 and sample capacitor area 14. For ease of drawing, a 6 x 6 pixel structure is shown but the array would typically be larger. Note how the output from each pixel is wired ("X" in Figure 8) to

a different conductor of the signal bus 10. Note also the cell width A of the system.

The embodiment of Figures 6 to 8 shows signal bus lines planar with the image plane, i.e. using the same conductor layer. One improvement (not shown) is to stack the conductors, that is to use different conductive layers. This reduces the amount of metal covering the pixel and thus improves the amount of light collected by the pixel.

The system described in Figure 6 is area and cost efficient but it suffers from "Fixed Pattern Noise" in the form of brightness variations on the picture. This is due to the varying amount of "threshold voltage" of transistors M1 over the array. These variations are a normal part of CMOS manufacturing process. A practical way of cancelling this offset is to measure, on a per-pixel basis, the reset voltage after the source follower.

Referring to Figures 9 and 10, this is achieved by closing switch S3 (Figure 9) immediately after the end of the reset pulse ("2" in Figure 10). This signal is then stored on "Cres" and switch S3 is opened. For a period of time ("3" in Figure 10), the pixel collects light and the photo-charge discharges the photodiode. At the end of this period ("4" in Figure 10) the signal is sampled on "Csn". During image readout ("5" in Figure 10), switches S2 and S4 are closed simultaneously and both the signal and

reset values are output onto the "Output Signal" and "Reset Value" conductors. The threshold voltage can then be compensated by subtracting the "Reset Value" from the "Output Signal".

This technique is similar to that used in US 5,122,881 but is modified to deal with the present situation where no multiplex transistor is present.

Although the technique described previously (Figure 9) cancels the offset, it degrades the rate at which the system can operate as it is not possible to perform image acquisition and readout simultaneously. This is because the reset signal ("2" in Figure 10) occurs at the start of an image acquisition, but is required during readout. A new acquisition is therefore not possible until readout has been completed.

The solution to this problem is shown in Figure 11. An extra capacitor per pixel is used to enable simultaneous image acquisition and readout.

To understand the operation of the circuit in Figure 11, refer to the timing diagram in Figure 12:

- At point "1", Vrst goes high causing all the M2s in the array to conduct, resetting the photodiodes in the array.

- As soon as this is complete, (point "2") S2 goes high enabling CresA to sample the reset value of the pixel.
- The image array collects light until time "3" when the voltage corresponding to the pixel's exposure to light is collected. S1 is closed and the voltage is stored on the pixel's Csn.

At this time the system has collected a complete set of reset and image values and is ready to readout. Before this occurs, the next acquisition cycle starts:

- At point "4", Vrst goes high causing all the M2s in the array to conduct, resetting the photodiodes in the array.
- As soon as this is complete, (point "5") S4 goes high enabling CresB to sample the reset value of the pixel.
- As the image array collects light, the pixels' capacitors are accessed sequentially. At point "6", S2 is closed to output the image value "Vsn" stored on Csn onto the "Output Signal" conductor. For this sequence of images, S4 is closed to output the reset value "Vres" stored on CresA onto the "Reset Value A" conductor.
- The image array collects light until time "7" when the voltage corresponding to the pixel's exposure to light is collected. S1 is closed and the voltage is stored on the pixel's Csn.

At this time the system has collected another complete set of reset and image values and is ready to readout. Before this occurs, the next acquisition cycle starts:

- Point "8" is identical to point "1"
- Point "9" is identical to point "2"
- As the image array collects light, the pixels' capacitors are accessed sequentially. At point "10", S2 is closed to output the image value "Vsn" stored on Csn onto the "Output Signal" conductor. For this sequence of images, S6 is closed to output the reset value "Vres" stored on CresB onto the "Reset Value B" conductor.

The system continues to operate using the sequence described above. The important feature to note on Figure 12 is that Vsn is able to be output on each frame.

In the layout shown in Figure 8, the pitch of the sample capacitors is 1/6th the pitch of the pixels as there are 6 pixels vertically. For a larger array, a greater number of sample capacitors needs to be fitted into the width of a pixel. This presents a practical limit to the architecture – the minimum width of sample capacitors is determined by the manufacturing technology used by the architecture, the maximum size of the pixel is determined by cost factors.

An improved layout is shown in Figure 13. This architecture has sample capacitors 14A and 14B at the top and bottom of the array 12. There are now two signal buses 10A and 10B, divided in the centre, and the cell width B is equal to 1/3 of a pixel. There are two advantages.

(1) The fewer signal bus conductors running across each pixel requires less metal and hence there is less obstruction of the pixel (i.e higher fill-factor) and hence greater sensitivity from the pixel.

(2) As the array is divided into two parts, the sample capacitors are shared top and bottom, resulting in twice the width available.

The following table illustrates the advantages:

Layout	Column Width	Pixel Array	Pixel Size	Image Plane	Imaging Area
Fig. 8	2μm	100x100	200μmx200μm	200mmx200mm	400m²
Fig. 13	2μm	100x100	100μmx100μm	100mmx10mm	100m²

As can be seen in the final column, the improved layout technique of Fig. 13 produces a four-fold increase in area (and hence a corresponding reduction in cost per unit area).

Turning to Figure 14, a preferred scheme for measuring and amplifying the two output signals will now be described.

Associated with the switches S2, S4, S6 and the conductors "Output Signal" 18, "Reset Value A" 20, and "Reset Value B" 22, are unwanted stray capacitances. As the array size increases, the number of pixels and therefore the number of switches increases. The cumulation of all these switches can produce an unwanted capacitance roughly equal to that of the sampling capacitances. When the signals are read out (switches S2/S4/S6 closed), part of the charge stored on the capacitors Csn/CresA/CresB is used to charge the stray capacitors. This problem is known as "charge sharing". This can easily be 50% to 70% of the signal, reducing the output swing to 1/2 or 1/4 of the "true" signal.

Using a differential, charge sensitive amplifier 16 as shown in Figure 14 charge sharing is avoided. Before the signal is read out, the switches S7, S8 are closed and the amplifier 16 put into its "common mode reset" state. This discharges the capacitors Cf1, Cf2 on the feedback of the operational amplifier 16 and forces the conductors 18, 20, 22 to the common mode voltage. Switches S7/S8 are opened and S2, S4 (or S6) are then closed. The nature of the operational amplifier is to ensure that its input remains at the common mode voltage. By doing so there is no change in voltage on the lines 18, 20 and

22 and so there can be no loss of charge. During the readout, the voltages on Csn, CresA, CresB are also set to the common mode voltage. The change in voltage from that which was measured off the array requires a current to flow. This comes from the output of the op-amp 16 via the feedback capacitors Cf1, Cf2. For correct (symmetrical operation) the capacitance of Cf1 = Cf2 and Csn=CresA=CresB. Hence:

$$Out1 - Out2=(Vsignal - Vreset)xCsn/Cf1$$

Modifications and improvements may be made to the foregoing within the scope of the invention.

Claims

1. A solid state imaging device comprising a two-dimensional array of pixels forming an image plane, and readout electronics for reading out signals from the pixels in a predetermined manner; and in which the readout electronics are located off said image plane.

2. The device of claim 1, in which each pixel is connected to its associated readout electronics via a multiconductor signal bus.

3. The device of Claim 2, in which each pixel comprises a photosensitive diode and switching means for resetting and discharging the diode; and in which the switching means consists only of a first transistor for applying a reset pulse and a second transistor operable to connect the diode to a predetermined conductor of said multi-conductor signal bus.

4. The device of Claim 2 or Claim 3, in which the signal bus conductors are stacked.

5. The device of any preceding Claim, in which the readout electronics are located at one side of the array.

6. The device of any one of Claims 1 to 5, in which the readout electronics are located on two opposite sides of the array.

7. The device of any preceding Claim, in which all pixels in the array are reset simultaneously and are read out simultaneously.

8. The device of any preceding Claim, in which the readout electronics comprises, for each pixel, a first store for a reset value and a second store for a read out value; and the readout electronics is effective to modify the read out value of a given pixel by the stored reset value for that pixel.

9. The device of Claim 8, in which the readout electronics further includes, for each pixel, a further store for a second reset value whereby the current reset and read out values may be processed simultaneously with applying a new reset pulse.

10. The device of Claim 9, in which the readout electronics further includes a differential amplifier connectable to said stores, and means for putting the amplifier into a common mode reset state prior to reading out a signal.

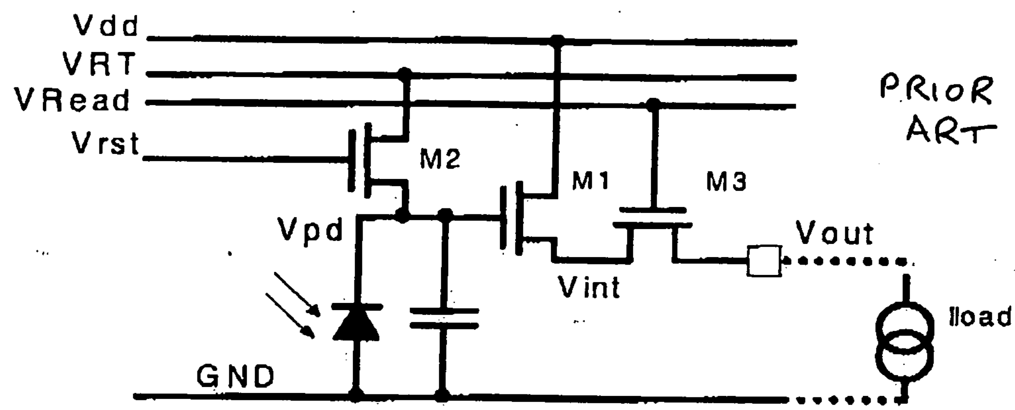


Figure 1 Three Transistor Pixel

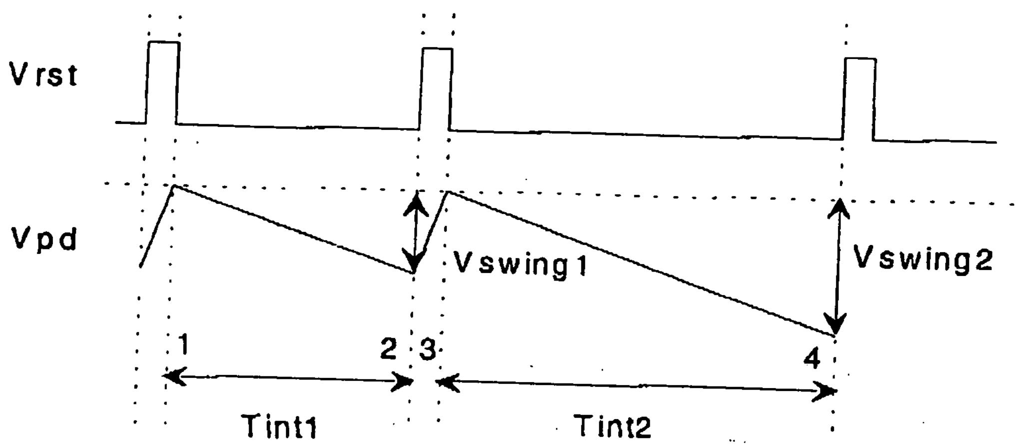
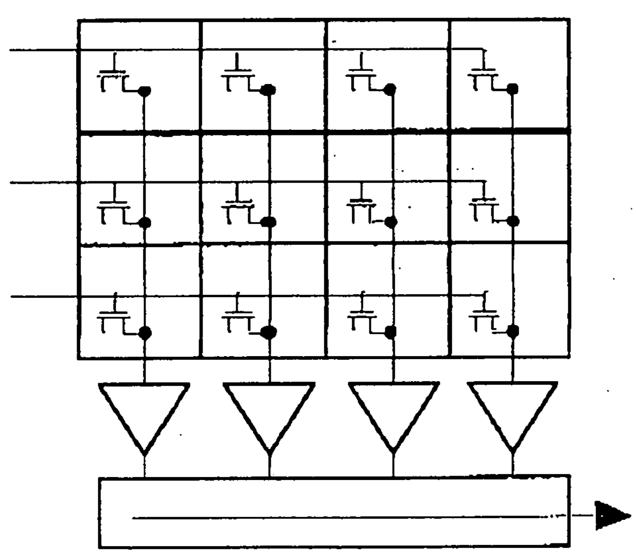


Figure 2 Voltage Swing on Photodiode



PRIOR ART

Figure 3 Multiplex Readout

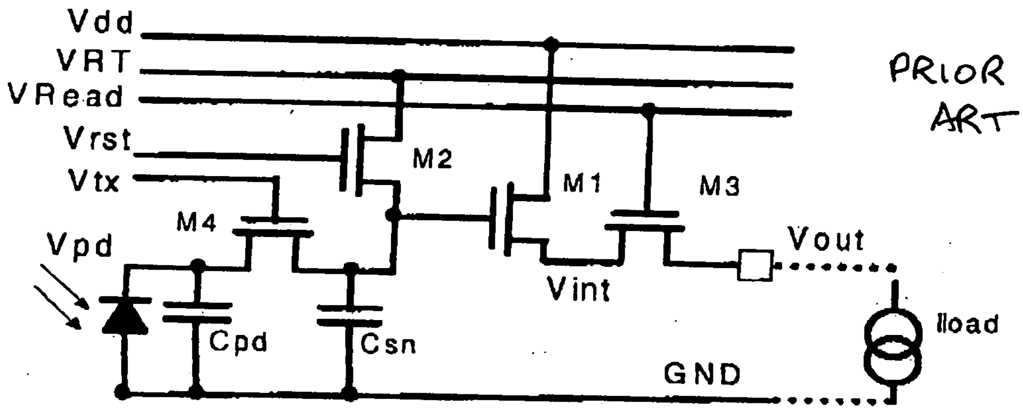


Figure 4 Four Transistor Pixel

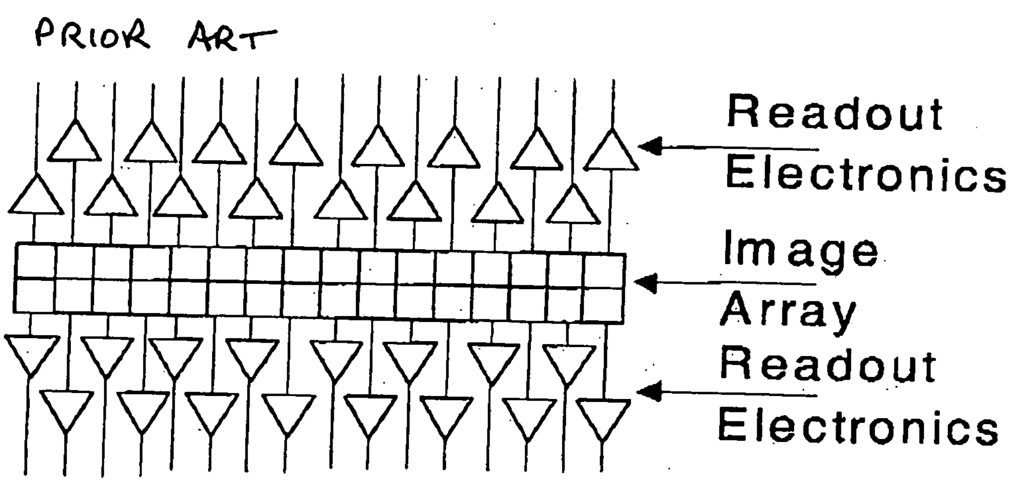


Figure 5 Sophisticated Linear Array

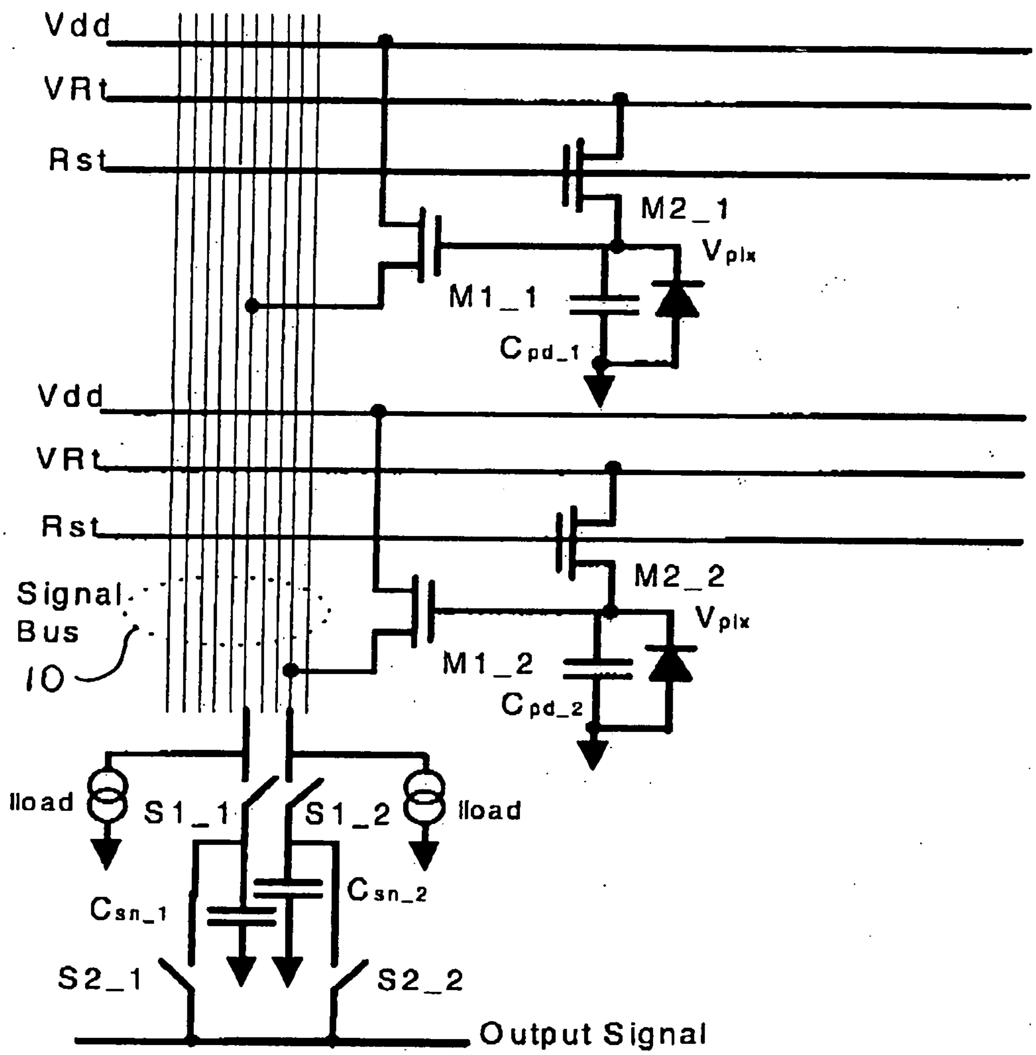


Figure 6 (Part of) New Column Structure

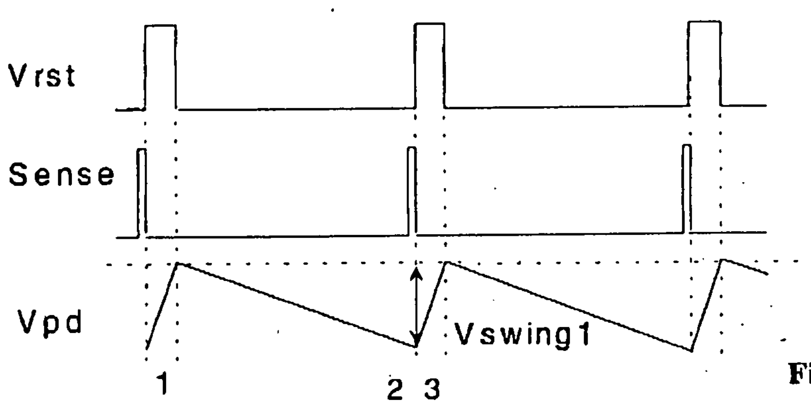


Figure 7 Timing Diagram

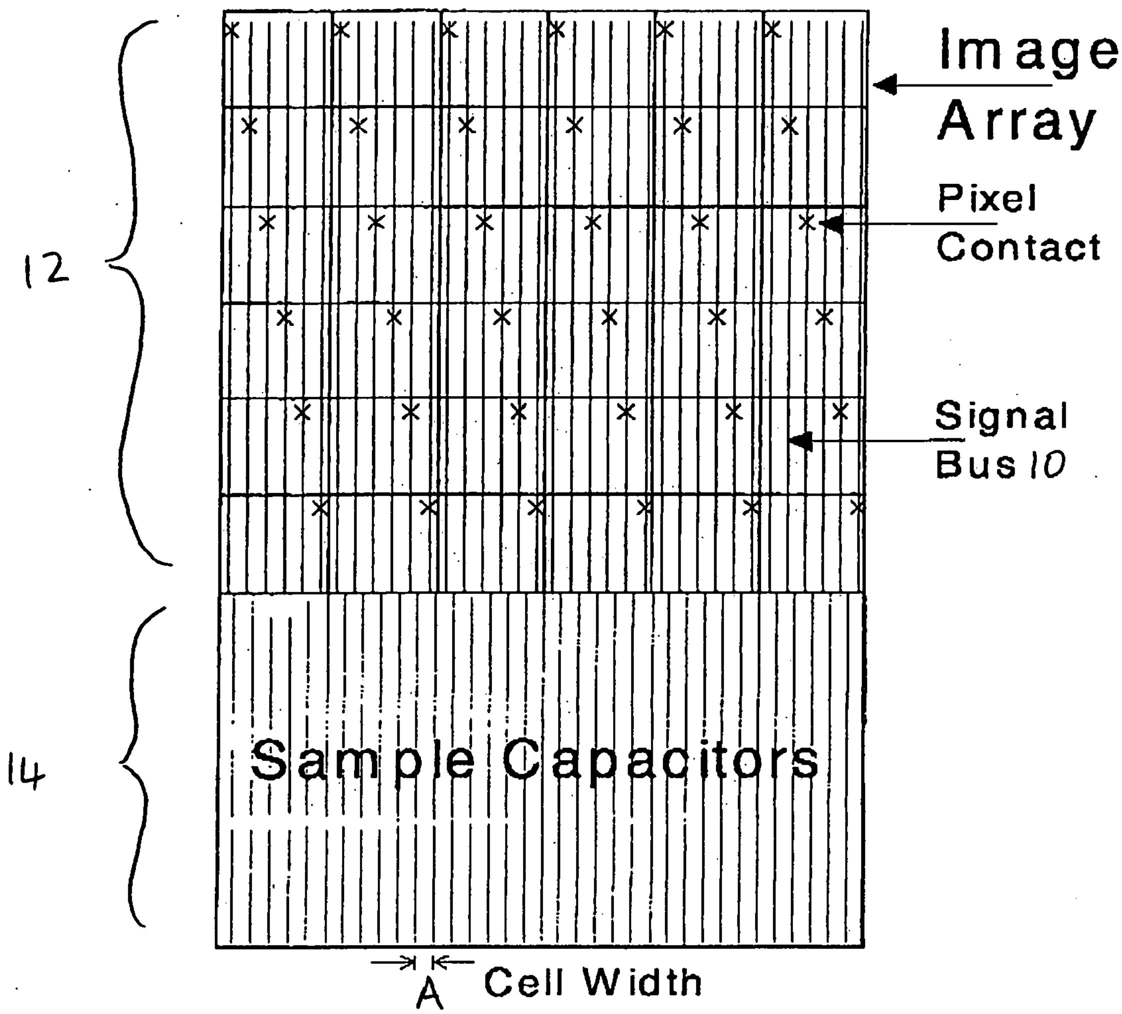


Figure 8 Typical System Layout

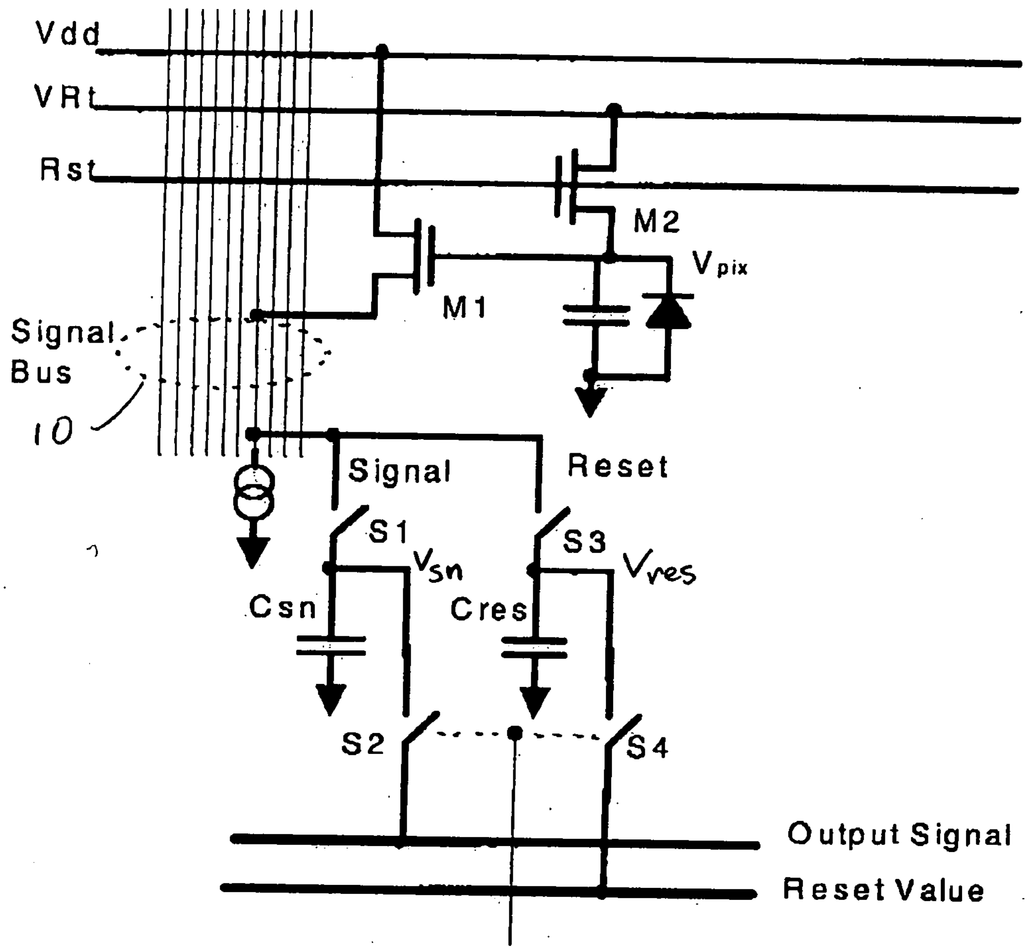


Figure 9 Improved Circuit - Offset Cancellation

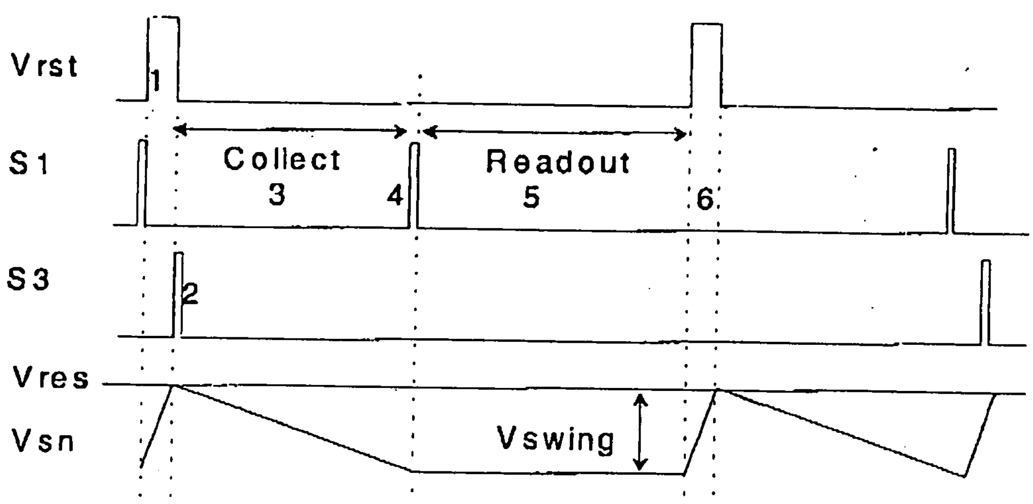


Figure 10 Offset Cancellation - Timing diagram

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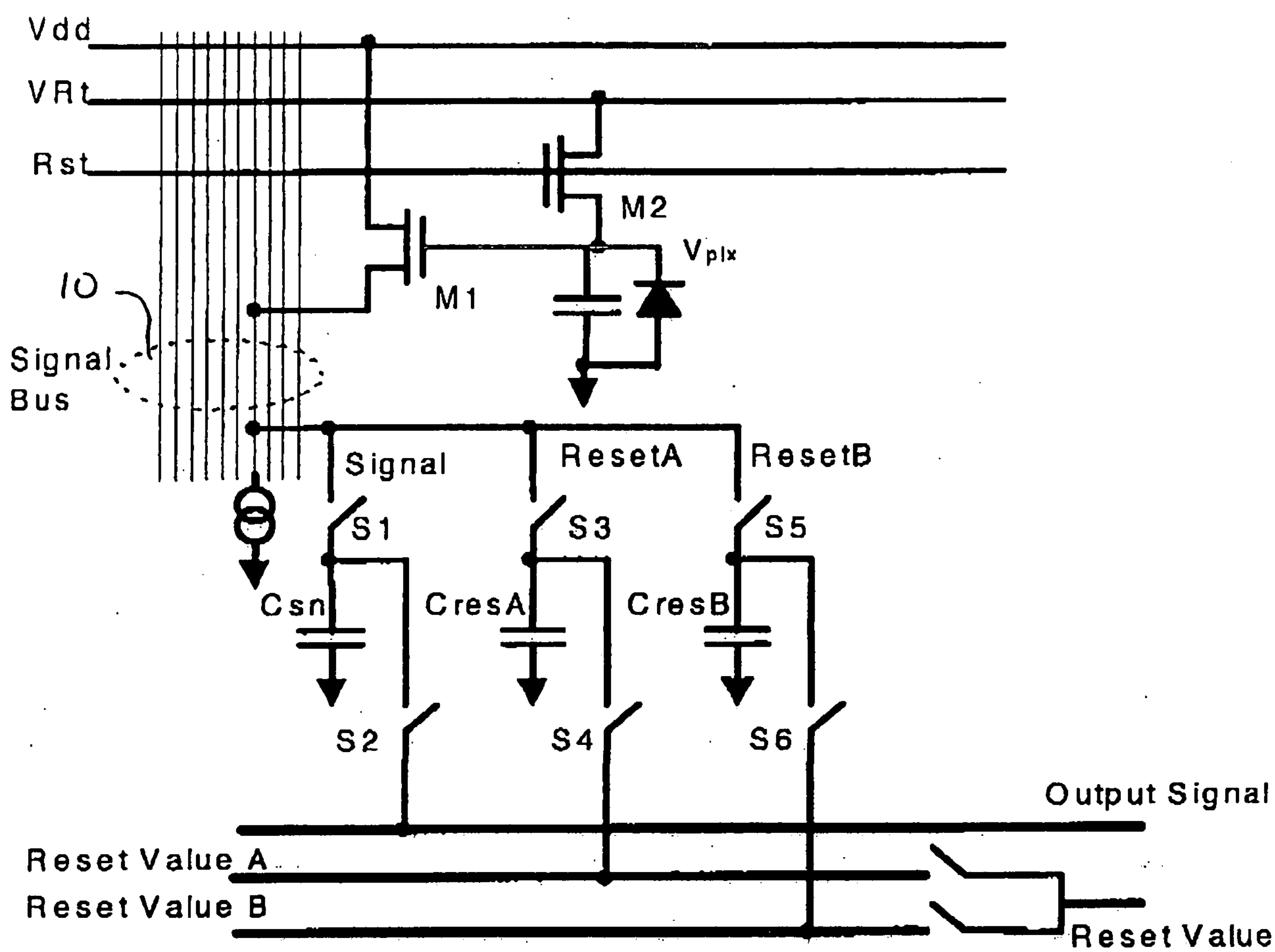

Figure 11 Improved Circuit - Offset Cancellation 2

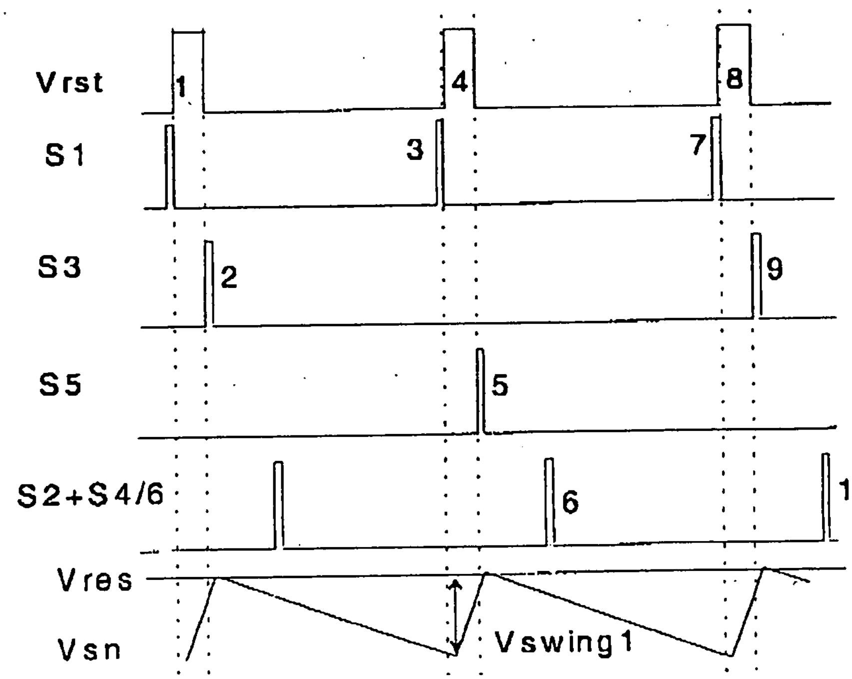

Figure 12 Offset Compensation 2 - Timing Diagram

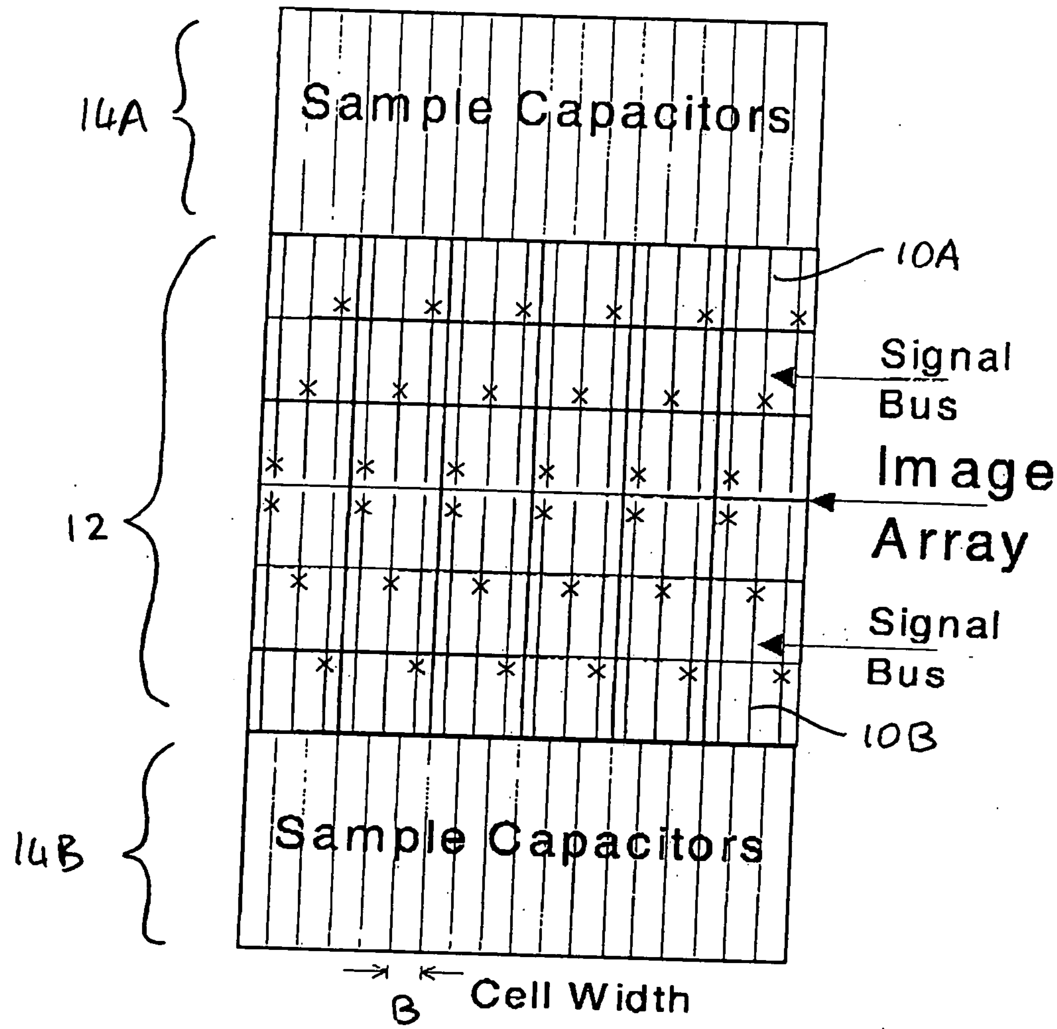

Figure 13 Improved Layout Technique

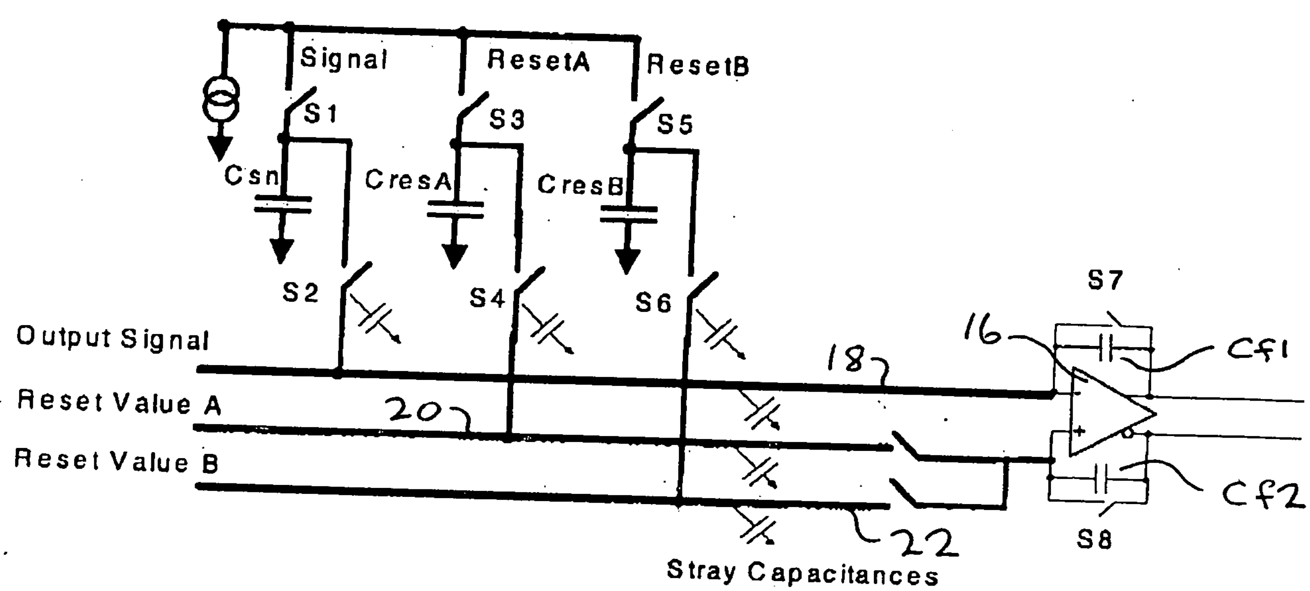

Figure 14 Preferred Readout Amplification